

USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: CLx Exit Timeouts

Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

Add timeouts to the first CLx Exit stages and allow not to report Logical Link Errors during the CLx Exit.
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Benefits as a result of the changes:

Increase clarity and improve interoperability.
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An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
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none

An analysis of the hardware implications:
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Routers may implement new additions.

An analysis of the software implications:
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None

An analysis of the compliance testing implications:
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none

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Actual Change

(a) Section 4.2.1.6.5.2 Gen 2 and Gen 3 Exit flow from CL1 or CL2 state (No Re-timers on the Link)

From Text:

This section applies when there are no USB4 Re-timers on the Link.

The USB4 Port initiating exit from CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS. If the receiver did not detect LFPS after $t_{\text{TrainingAbort2}}$ time the Router shall initiate a Disconnect by driving SBTX to a logical low state for $t_{\text{DisconnectTx}}$.
2. Return to Electrical Idle for t_{PreData} .
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than $t_{\text{CLxIdleRx}}$ after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within t_{RxLock} time.
5. Transition the Lane Adapter to Training.LOCK1 sub-state.
 - On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.

To Text:

This section applies when there are no USB4 Re-timers on the Link.

The USB4 Port initiating exit from CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until the receiver detects LFPS. If the receiver did not detect LFPS after $t_{\text{TrainingAbort2}}$ time the Router shall initiate a Disconnect by driving SBTX to a logical low state for $t_{\text{DisconnectTx}}$.
2. Return to Electrical Idle for t_{PreData} .
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than $t_{\text{CLxIdleRx}}$ after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within t_{RxLock} time.
5. Transition the Lane Adapter to Training.LOCK1 sub-state.
 - On transition to the TS1 sub-state, the USB4 Port shall enable SSC if SSC is disabled.

If the Adapter did not reach Training.LOCK1 sub-state $t_{\text{TrainingAbort2}}$ time after LFPS transmission has started, the Router should initiate a Disconnect by driving SBTX to a logical low state for $t_{\text{DisconnectTx}}$.

Implementation Note: a single $t_{\text{TrainingAbort2}}$ Timer used for step 1 and up to step 5 can be implemented.

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(b) Section 4.2.1.6.5.3 Gen 2 and Gen 3 Exit flow from CL1 or CL2 state (Re-timers on the Link)

From Text:

This section applies when there is at least one USB4 Re-timer on the Link.

The USB4 Port initiating exit from CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS. If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
2. Return to Electrical Idle for tPreData.
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The first CL_WAKE2.X Ordered Set Symbol shall be sent within tWakeResponse after receiving the third CL_WAKE1.X Ordered Set Symbol. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Ordered Set Symbols interleaved with CL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set Symbols. If the receiver loses Symbol alignment lock after the transmitter sends the CL_WAKE2.X Ordered Set, the receiver shall regain Symbol alignment lock within tSymbolLock time.
6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition the Adapter to Training.LOCK1 sub-state within tWakeResponse time.

To Text:

This section applies when there is at least one USB4 Re-timer on the Link.

The USB4 Port initiating exit from CL1 or CL2 state shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst on each Lane until its receiver detects LFPS. If the receiver did not detect LFPS after tTrainingAbort2 time the Router shall initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.
2. Return to Electrical Idle for tPreData.
3. Start transmitting SLOS1 on the Lane.
 - A USB4 Port may exit CL2 or CL1 state with SSC enabled or disabled.
4. Enable the receiver to start bit and symbol synchronization not earlier than tCLxIdleRx after the last LFPS cycle received. A Lane Adapter shall complete Symbol lock within tRxLock time.
5. Upon reception of 3 back-to-back CL_WAKE1.X Ordered Set Symbols, start transmitting CL_WAKE2.X Ordered Set Symbols on the Lane. The first CL_WAKE2.X Ordered Set Symbol shall be sent within tWakeResponse after receiving the third CL_WAKE1.X Ordered Set Symbol. The Adapter shall ignore any received CL_WAKE2.Y (where Y is any value) Ordered Set Symbols interleaved with CL_WAKE1.X Ordered Set Symbols when it determines the reception of back-to-back CL_WAKE1.X Ordered Set Symbols. If the receiver loses Symbol alignment lock after the transmitter sends the CL_WAKE2.X Ordered Set, the receiver shall regain Symbol alignment lock within tSymbolLock time.
6. Upon reception of 7 back-to-back CL_WAKE2.X Ordered Set Symbols or 7 back-to-back SLOS Symbols, transition the Adapter to Training.LOCK1 sub-state within tWakeResponse time.

If the Adapter did not reach Training.LOCK1 sub-state tTrainingAbort2 time after LFPS transmission has started, the Router should initiate a Disconnect by driving SBTX to a logical low state for tDisconnectTx.

Implementation Note: a single tTrainingAbort2 Timer used for step 1 and up to step 6 can be implemented.

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(c) Section Table 4-72. Logical Layer Timing Parameters

From Text:

Parameter	Description	Min	Max	Units
tTrainingAbort2	<ol style="list-style-type: none"> 1. The amount of time in Training state following any transition to Training state other than from CLd state. 2. The time to send LFPS when exiting CL1 or CL2 or exiting CL0s for Gen 4. 3. The time to send SLOS1 in CL0s exit. 	100	--	ms

To Text:

Parameter	Description	Min	Max	Units
tTrainingAbort2	<ol style="list-style-type: none"> 1. The amount of time in Training state following any transition to Training state other than from CLd state. 2. The time to send LFPS when exiting CL1 or CL2 or exiting CL0s for Gen 4. 3. The time to send SLOS1 in CL0s exit. 4. The amount of time in CLx Exit from LFPS transmission to either detecting LFPS or reaching Training.LOCK1 substate for Gen2/3. 	100	--	ms

(d) Table 4-66. Error Cases and Impact on Logical Layer

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From Text:

Error	Event	Response	Reporting
Alignment Lock Error (ALE)	Adapter received N number of Symbols in a row with illegal Sync Bits values, where N is a number between 1 and 8 (inclusive) that is chosen by the implementation.	Go to Training.LOCK1 sub-state. During Gen 2 and Gen 3 CLx exit when re-timers are present on the link, an adapter may continue to lock on CL_WAKE1.X till tTrainingAbort2 timeout. See Section 4.2.1.6.5.3.	An Adapter shall set the <i>ALE</i> bit in the <i>Logical Layer Errors</i> field to 1b. If the <i>ALE</i> bit in the <i>Logical Layer Errors Enable</i> field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5). If the <i>ALE</i> bit in the <i>Logical Layer Errors Enable</i> field is 0b, the Router shall not send a Notification Packet.
Order Set Error (OSE)	Gen 2/3 – Adapter received 2 back-to-back Symbols that contain an Ordered Set that is not defined in this specification and/or have an uncorrectable error in the <i>SCR</i> field. Gen 4 – Control Symbols received in a way that doesn't match any Ordered Set.	Gen 2/3 – Go to Training.LOCK1 sub-state. During Gen 2 and Gen 3 CLx exit when re-timers are present on the link, an adapter may continue to lock on CL_WAKE1.X till tTrainingAbort2 timeout. See Section 4.2.1.6.5.3.	An Adapter shall set the <i>OSE</i> bit in the <i>Logical Layer Errors</i> field to 1b. If the <i>OSE</i> bit in the <i>Logical Layer Errors Enable</i> field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5). If the <i>OSE</i> bit in the <i>Logical Layer Errors Enable</i> field is 0b, the Router shall not send a Notification Packet.
Timeout Error (TE)	Adapter entered Training state from either CL0, CL1, or CL2 state and did not transition to CL0 state within tTrainingError after sending the first SLOS1 (in Gen 2/3) or Gen 4 TS1 (in Gen 4).	Gen 2/3 – Go to Training.LOCK1 sub-state. Gen 4 – Initiate Gen 4 Link Recovery (see Section 4.4.7).	An Adapter shall set the <i>TE</i> bit in the <i>Logical Layer Errors</i> field to 1b. If the <i>TE</i> bit in the <i>Logical Layer Errors Enable</i> field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5). If the <i>TE</i> bit in the <i>Logical Layer Errors Enable</i> field is 0b, the Router shall

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			not send a Notification Packet.
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To Text:

Error	Event	Response	Reporting
Alignment Lock Error (ALE)	Adapter received N number of Symbols in a row with illegal Sync Bits values, where N is a number between 1 and 8 (inclusive) that is chosen by the implementation.	Go to Training.LOCK1 sub-state. During Gen 2 and Gen 3 CLx exit when re-timers are present on the link, an adapter may continue to lock on CL_WAKE1.X till tTrainingAbort2 timeout. See Section 4.2.1.6.5.3.	During Gen2 and Gen3 CLx Exit when re-timers are present on the link, an Adapter may ignore the ALE errors and not report them. Otherwise, an Adapter may set the ALE bit in the Logical Layer Errors field to 1b. If the ALE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5). If the ALE bit in the Logical Layer Errors Enable field is 0b, the Router shall not send a Notification Packet.
Order Set Error (OSE)	Gen 2/3 – Adapter received 2 back-to-back Symbols that contain an Ordered Set that is not defined in this specification and/or have an uncorrectable error in the SCR field. Gen 4 – Control Symbols received in a way that doesn't match any Ordered Set.	Gen 2/3 – Go to Training.LOCK1 sub-state. During Gen 2 and Gen 3 CLx exit when re-timers are present on the link, an adapter may continue to lock on CL_WAKE1.X till tTrainingAbort2 timeout. See Section 4.2.1.6.5.3.	During Gen2 and Gen3 CLx Exit when re-timers are present on the link, an Adapter may ignore the OSE errors and not report them. Otherwise, an Adapter shall set the OSE bit in the Logical Layer Errors field to 1b. If the OSE bit in the Logical Layer Errors Enable field is 1b, the Router shall send a

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			Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5). If the <i>OSE</i> bit in the <i>Logical Layer Errors Enable</i> field is 0b, the Router shall not send a Notification Packet.
Timeout Error (TE)	Adapter entered Training state from either CL0, CL1, or CL2 state and did not transition to CL0 state within tTrainingError after sending the first SLOS1 (in Gen 2/3) or Gen 4 TS1 (in Gen 4).	Gen 2/3 – Go to Training.LOCK1 sub-state. Gen 4 – Initiate Gen 4 Link Recovery (see Section 4.4.7).	An Adapter shall set the <i>TE</i> bit in the <i>Logical Layer Errors</i> field to 1b. If the <i>TE</i> bit in the <i>Logical Layer Errors Enable</i> field is 1b, the Router shall send a Notification Packet with Event Code = ERR_LINK to the Connection Manager (see Section 6.5). If the <i>TE</i> bit in the <i>Logical Layer Errors Enable</i> field is 0b, the Router shall not send a Notification Packet.